

IEEE JOURNAL OF SOLID-STATE CIRCUITS

A PUBLICATION OF THE IEEE SOLID-STATE CIRCUITS SOCIETY



DECEMBER 2010

VOLUME 45

NUMBER 12

IJSCBC

(ISSN 0018-9200)

SPECIAL ISSUE ON THE 2010 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE (ISSCC)

New Associate Editors	<i>U. Moon</i>	2503
Introduction to the Special Issue on the 2010 IEEE International Solid-State Circuits Conference	<i>G.-H. Cho, B. Murmann, K. Halonen, R. Gharpurey, and J.-Y. Sim</i>	2505
<hr/>		
A Thermal-Diffusivity-Based Frequency Reference in Standard CMOS With an Absolute Inaccuracy of $\pm 0.1\%$ From -55°C to 125°C	<i>S. M. Kashmiri, M. A. P. Pertijs, and K. A. A. Makinwa</i>	2510
A Micropower Chopper—CDS Operational Amplifier	<i>M. Belloni, E. Bonizzoni, A. Fornasari, and F. Maloberti</i>	2521
A Class-G Headphone Amplifier in 65 nm CMOS Technology	<i>A. Lollo, G. Bollati, and R. Castello</i>	2530
A Two-Phase Switching Hybrid Supply Modulator for RF Power Amplifiers With 9% Efficiency Improvement	<i>P. Y. Wu and P. K. T. Mok</i>	2543
A Fully-Integrated Switched-Capacitor Step-Down DC-DC Converter With Digital Capacitance Modulation in 45 nm CMOS	<i>Y. K. Ramadass, A. A. Fayed, and A. P. Chandrakasan</i>	2557
A Low Area, Switched-Resistor Based Fractional-N Synthesizer Applied to a MEMS-Based Programmable Oscillator ..	<i>M. H. Perrott, S. Pamarti, E. G. Hoffman, F. S. Lee, S. Mukherjee, C. Lee, V. Tsinker, S. Perumal, B. T. Soto, N. Arumugam, and B. W. Garlepp</i>	2566
A 2.1-to-2.8-GHz Low-Phase-Noise All-Digital Frequency Synthesizer With a Time-Windowed Time-to-Digital Converter	<i>T. Tokairin, M. Okada, M. Kitsunezuka, T. Maeda, and M. Fukaiishi</i>	2582
A 1.2-V 10- μW NPN-Based Temperature Sensor in 65-nm CMOS With an Inaccuracy of 0.2°C (3σ) From -70°C to 125°C	<i>F. Sebastiano, L. J. Breems, K. A. A. Makinwa, S. Drago, D. M. W. Leenaerts, and B. Nauta</i>	2591
A 16-bit 250-MS/s IF Sampling Pipelined ADC With Background Calibration	<i>A. M. A. Ali, A. Morgan, C. Dillon, G. Patterson, S. Puckett, P. Bhoraskar, H. Dinc, M. Hensley, R. Stop, S. Bardsley, D. Lattimore, J. Bray, C. Speir, and R. Sneed</i>	2602
A 16-Bit 100 to 160 MS/s SiGe BiCMOS Pipelined ADC With 100 dBFS SFDR	<i>R. Payne, M. Corsi, D. Smith, T.-L. Hsieh, and S. Kaylor</i>	2613
Design of a Split-CLS Pipelined ADC With Full Signal Swing Using an Accurate But Fractional Signal Swing Opamp ..	<i>B. Hershberg, S. Weaver, and U. Moon</i>	2623
A Mostly-Digital Variable-Rate Continuous-Time Delta-Sigma Modulator ADC	<i>G. Taylor and I. Galton</i>	2634

(Contents Continued on Page 2502)



An 18 b 12.5 MS/s ADC With 93 dB SNR	<i>C. P. Hurrell, C. Lyden, D. Laing, D. Hummerston, and M. Vickery</i>	2647
A Millimeter-Wave Intra-Connect Solution	<i>K. Kawasaki, Y. Akiyama, K. Komori, M. Uno, H. Takeuchi, T. Itagaki, Y. Hino, Y. Kawasaki, K. Ito, and A. Hajimiri</i>	2655
A 90 GHz Hybrid Switching Pulsed-Transmitter for Medical Imaging	<i>A. Arbabian, S. Callender, S. Kang, B. Afshar, J.-C. Chien, and A. M. Niknejad</i>	2667
A 60-GHz Band 2×2 Phased-Array Transmitter in 65-nm CMOS	<i>W. L. Chan and J. R. Long</i>	2682
A Passive Mixer-First Receiver With Digitally Controlled and Widely Tunable RF Interface	<i>C. Andrews and A. C. Molnar</i>	2696
A CMOS Broadband Power Amplifier With a Transformer-Based High-Order Output Matching Network	<i>H. Wang, C. Sideris, and A. Hajimiri</i>	2709
A 3.5 GHz Wideband ADPLL With Fractional Spur Suppression Through TDC Dithering and Feedforward Compensation	<i>E. Temporiti, C. Weltin-Wu, D. Baldi, M. Cusmai, and F. Svelto</i>	2723
Capacitive Degeneration in LC-Tank Oscillator for DCO Fine-Frequency Tuning	<i>L. Fanori, A. Liscidini, and R. Castello</i>	2737
A Fully-Integrated 77-GHz FMCW Radar Transceiver in 65-nm CMOS Technology	<i>J. Lee, Y.-A. Li, M.-H. Hung, and S.-J. Huang</i>	2746
A Fully Integrated 16-Element Phased-Array Transmitter in SiGe BiCMOS for 60-GHz Communications	<i>A. Valdes-Garcia, S. T. Nicolson, J.-W. Lai, A. Natarajan, P.-Y. Chen, S. K. Reynolds, J.-H. C. Zhan, D. G. Kam, D. Liu, and B. Floyd</i>	2757
A Fully Integrated 2×1 Dual-Band Direct-Conversion Mobile WiMAX Transceiver With Dual-Mode Fractional Divider and Noise-Shaping Transimpedance Amplifier in 65 nm CMOS	<i>J. Deguchi, D. Miyashita, Y. Ogasawara, G. Takemura, M. Iwanaga, K. Sami, R. Ito, J. Wadatsumi, Y. Tsuda, S. Oda, S. Kawaguchi, N. Itoh, and M. Hamada</i>	2774
A 10-MHz Signal Bandwidth Cartesian Loop Transmitter Capable of Off-Chip PA Linearization	<i>H. Ishihara, M. Hosoya, S. Otaka, and O. Watanabe</i>	2785
A 5 mm^2 40 nm LP CMOS Transceiver for a Software-Defined Radio Platform	<i>M. Ingels, V. Giannini, J. Borremans, G. Mandal, B. Debaillie, P. Van Wesemael, T. Sano, T. Yamamoto, D. Hauspie, J. Van Driessche, and J. Craninckx</i>	2794
A 900-MHz Direct Delta-Sigma Receiver in 65-nm CMOS	<i>K. Koli, S. Kallioinen, J. Jussila, P. Sivonen, and A. Pärssinen</i>	2807
A Calibration-Free 800 MHz Fractional-N Digital PLL With Embedded TDC	<i>M. S.-W. Chen, D. Su, and S. Mehta</i>	2819
A $47 \times 10 \text{ Gb/s}$ 1.4 mW/Gb/s Parallel Interface in 45 nm CMOS	<i>F. O'Mahony, J. E. Jaussi, J. Kennedy, G. Balamurugan, M. Mansuri, C. Roberts, S. Shekhar, R. Mooney, and B. Casper</i>	2828
A 12.3-mW 12.5-Gb/s Complete Transceiver in 65-nm CMOS Process	<i>K. Fukuda, H. Yamashita, G. Ono, R. Nemoto, E. Suzuki, N. Masuda, T. Takemoto, F. Yuki, and T. Saito</i>	2838
A 4.5 mW/Gb/s 6.4 Gb/s $22+1$ -Lane Source Synchronous Receiver Core With Optional Cleanup PLL in 65 nm CMOS ..	<i>R. Reutemann, M. Ruegg, F. Keyser, J. Bergkvist, D. Dreps, T. Toifl, and M. Schmatz</i>	2850
An 8.5-Gb/s Fully Integrated CMOS Optoelectronic Receiver Using Slope-Detection Adaptive Equalizer	<i>D. Lee, J. Han, G. Hañ, and S. M. Park</i>	2861
A 1 GHz ADPLL With a 1.25 ps Minimum-Resolution Sub-Exponent TDC in $0.18 \mu\text{m}$ CMOS	<i>S.-K. Lee, Y.-H. Seo, H.-J. Park, and J.-Y. Sim</i>	2874
2010 INDEX		2883