

IEEE JOURNAL OF SOLID-STATE CIRCUITS

上海理工大学图书馆
军工路516号邮编:200093

A PUBLICATION OF THE IEEE SOLID-STATE CIRCUITS SOCIETY



APRIL 2011

VOLUME 46

NUMBER 4

IJSCBC

(ISSN 0018-9200)

SPECIAL ISSUE ON THE 2010 SYMPOSIUM ON VLSI CIRCUITS

Introduction to the Special Issue on the 2010 Symposium on VLSI Circuits A. Amerasekera and M. Nagata 719

PAPERS

- Microwatt Embedded Processor Platform for Medical System-on-Chip Applications S. R. Sridhara, M. DiRenzo, S. Lingam, S.-J. Lee, R. Blázquez, J. Maxey, S. Ghanem, Y.-H. Lee, R. Abdallah, P. Singh, and M. Goel 721
- A Battery-Powered Activity-Dependent Intracortical Microstimulation IC for Brain-Machine-Brain Interface M. Azin, D. J. Guggenmos, S. Barbay, R. J. Nudo, and P. Mohseni 731
- A Biomedical Sensor Interface With a *sinc* Filter and Interference Cancellation J. L. Bohorquez, M. Yip, A. P. Chandrakasan, and J. L. Dawson 746
- A 2 Tb/s 6×4 Mesh Network for a Single-Chip Cloud Computer With DVFS in 45 nm CMOS P. Salihundam, S. Jain, T. Jacob, S. Kumar, V. Erraguntla, Y. Hoskote, S. Vangal, G. Ruhl, and N. Borkar 757
- 53 Gbps Native GF(2⁴)² Composite-Field AES-Encrypt/Decrypt Accelerator for Content-Protection in 45 nm High-Performance Microprocessors S. K. Mathew, F. Sheikh, M. Kounavis, S. Gueron, A. Agarwal, S. K. Hsu, H. Kaul, M. A. Anders, and R. K. Krishnamurthy 767
- A 530 Mpixels/s 4096x2160@60fps H.264/AVC High Profile Video Decoder Chip D. Zhou, J. Zhou, X. He, J. Zhu, J. Kong, P. Liu, and S. Goto 777
- An On-Chip Waveform Capturer and Application to Diagnosis of Power Delivery in SoC Integration T. Hashida and M. Nagata 789
- Tunable Replica Bits for Dynamic Variation Tolerance in 8T SRAM Arrays A. Raychowdhury, B. M. Geuskens, K. A. Bowman, J. W. Tschanz, S.-L. L. Lu, T. Karnik, M. M. Khellah, and V. K. De 797
- Multi-Step Word-Line Control Technology in Hierarchical Cell Architecture for Scaled-Down High-Density SRAMs .. K. Takeda, T. Saito, S. Asayama, Y. Aimoto, H. Kobatake, S. Ito, T. Takahashi, M. Nomura, K. Takeuchi, and Y. Hayashi 806
- A Large $\sigma V_{TH}/VDD$ Tolerant Zigzag 8T SRAM With Area-Efficient Decoupled Differential Sensing and Fast Write-Back Scheme J.-J. Wu, Y.-H. Chen, M.-F. Chang, P.-W. Chou, C.-Y. Chen, H.-J. Liao, M.-B. Chen, Y.-H. Chu, W.-C. Wu, and H. Yamauchi 815

1-Tbyte/s 1-Gbit DRAM Architecture Using 3-D Interconnect for High-Throughput Computing	<i>T. Sekiguchi, K. Ono, A. Kotabe, and Y. Yanagawa</i>	828
A 12-GS/s 81-mW 5-bit Time-Interleaved Flash ADC With Background Timing Skew Calibration	<i>M. El-Chammas and B. Murmann</i>	838
A CMOS 6-Bit 16-GS/s Time-Interleaved ADC Using Digital Background Calibration Techniques	<i>C.-C. Huang, C.-Y. Wang, and J.-T. Wu</i>	848
A SAR-Assisted Two-Stage Pipeline ADC	<i>C. C. Lee and M. P. Flynn</i>	859
A Quad-Band GSM/GPRS/EDGE SoC in 65 nm CMOS	<i>H. Darabi, P. Chang, H. Jensen, A. Zolfaghari, P. Lettieri, J. C. Leete, B. Mohammadi, J. Chiu, Q. Li, S. Chen, Z. Zhou, M. Vadipour, C. Chen, Y. Chang, A. Mirzaei, A. Yazdi, M. Nariman, A. Hadji-Abdolhamid, E. Chang, B. Zhao, K. Juan, P. Suri, C. Guan, L. Serrano, J. Leung, J. Shin, J. Kim, H. Tran, P. Kilcoyne, H. Vinh, E. Raith, M. Koscal, A. Hukkoo, C. Hayek, V. Rakhshani, C. Wilcoxson, M. Rofougaran, and A. Rofougaran</i>	870
A Novel Variable Inductor Using a Bridge Circuit and Its Application to a 5–20 GHz Tunable LC-VCO	<i>A. Tanabe, K. Hijioka, H. Nagase, and Y. Hayashi</i>	883
A 300-GHz Fundamental Oscillator in 65-nm CMOS Technology	<i>B. Razavi</i>	894
Interleaving Energy-Conservation Mode (IECM) Control in Single-Inductor Dual-Output (SIDO) Step-Down Converters With 91% Peak Efficiency	<i>Y.-H. Lee, Y.-Y. Yang, S.-J. Wang, K.-H. Chen, Y.-H. Lin, Y.-K. Chen, and C.-C. Huang</i>	904
A 112 Mb/s Full Duplex Remotely-Powered Impulse-UWB RFID Transceiver for Wireless NV-Memory Applications ..	<i>M. Pelissier, J. Jantunen, B. Gomez, J. Arponen, G. Masson, S. Dia, J. Varteva, and M. Gary</i>	916
A Low Energy Injection-Locked FSK Transceiver With Frequency-to-Amplitude Conversion for Body Sensor Applications	<i>J. Bae, L. Yan, and H.-J. Yoo</i>	928
A 250 mV, 352 μ W GPS Receiver RF Front-End in 130 nm CMOS	<i>A. Heiberg, T. Brown, T. Fiez, and K. Mayaram</i>	938
A 65 nm CMOS Quad-Band SAW-Less Receiver SoC	<i>A. Mirzaei, H. Darabi, A. Yazdi, Z. Zhou, E. Chang, and P. Suri</i>	950
A 0.55 V 10 fJ/bit Inductive-Coupling Data Link and 0.7 V 135 fJ/Cycle Clock Link With Dual-Coil Transmission Scheme	<i>N. Miura, T. Shidei, Y. Yuan, S. Kawai, K. Takatsu, Y. Kiyota, Y. Asano, and T. Kuroda</i>	965
A 5 Gb/s Link With Matched Source Synchronous and Common-Mode Clocking Techniques	<i>J. Zerbe, B. Daly, L. Luo, W. Stonecipher, W. Dettloff, J. C. Eble, T. Stone, J. Ren, B. Leibowitz, M. Bucher, P. Satarzadeh, Q. Lin, Y. Lu, and R. Kollipara</i>	974
An Ultra-Wide Range Bi-Directional Transceiver With Adaptive Power Control Using Background Replica VCO Gain Calibration	<i>T. Ebuchi, Y. Komatsu, M. Miura, T. Chiba, T. Iwata, S. Doshio, and T. Yoshikawa</i>	986