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Introduction to the 31st Annual IEEE Compound Semiconductor Integrated Circuit Symposium *M. Sokolich and T. Dickson* 1959

PAPERS

- A 120–145 GHz Heterodyne Receiver Chipset Utilizing the 140 GHz Atmospheric Window for Passive Millimeter-Wave Imaging Applications *S. Koch, M. Guthoerl, I. Kallfass, A. Leuther, and S. Saito* 1961
- An 18-Gb/s, Direct QPSK Modulation SiGe BiCMOS Transceiver for Last Mile Links in the 70–80 GHz Band *I. Sarkas, S. T. Nicolson, A. Tomkins, E. Laskin, P. Chevalier, B. Sautreuil, and S. P. Voinigescu* 1968
- A Passive W-Band Imaging Receiver in 65-nm Bulk CMOS *A. Tomkins, P. Garcia, and S. P. Voinigescu* 1981
- A 0.25 μm InP DHBT 200 GHz+ Static Frequency Divider *M. D'Amore, C. Monier, S. T. Lin, B. Oyama, D. W. Scott, E. N. Kaneshiro, P.-C. Chang, K. F. Sato, A. Niemi, L. Dang, A. Cavus, A. Gutierrez-Aitken, and A. K. Oki* 1992
- A Low-Loss 50–70 GHz SPDT Switch in 90 nm CMOS *M. Uzunkol and G. M. Rebeiz* 2003
- MMIC LNAs for Radioastronomy Applications Using Advanced Industrial 70 nm Metamorphic Technology *W. Ciccognani, E. Limiti, P. E. Longhi, and M. Renvoisè* 2008
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